Claim 2 stood rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang et al.

These rejections are respectfully traversed and reconsideration is respectfully requested.

The Present Invention

The present invention, as clearly recited in new claims 6-9, provides a wafer that includes, among other things, a first titanium layer on a non-passivated die at non-isolation locations. A copper layer is directly on the first titanium layer while a titanium passivation layer is directly on the copper layer at non-solder bump locations. Under bump material is provided directly on the copper layer at the bump locations. Claims 8 and 9 are directed to a chip device that includes such a wafer. Thus, the present invention provides a wafer that includes a titanium passivation layer. Titanium tends to passivate itself and adheres well to copper as well as aluminum, thereby forming a good interlayer. Solder does not wet the titanium layer, thus providing for defined solderable surfaces on the wafer.

The Cited References

In contrast to the present invention, Wang et al. disclose using the titanium and copper layers to provide barrier layers. No disclosure or suggestion is even made about using titanium as a passivation layer. No suggestion is even made with regard to providing titanium and copper layers along with under bump material at solder bump locations, and then providing a titanium layer with a copper layer directly thereon along with a titanium passivation layer directly on the copper layer at non-isolation points of the wafer.

Likewise, Mizuhara et al. disclose using the titanium and copper layers as barrier metals, thus providing insulating layers. Once again, no mention or suggestion is

made of providing a titanium layer with a copper layer directly thereon with under bump material on the copper layer at solder bump locations, and providing a titanium layer with a copper layer directly thereon and a titanium passivation layer directly on the copper layer at non-isolation locations.

Accordingly, it is respectfully submitted that claims 6-9 are allowable.

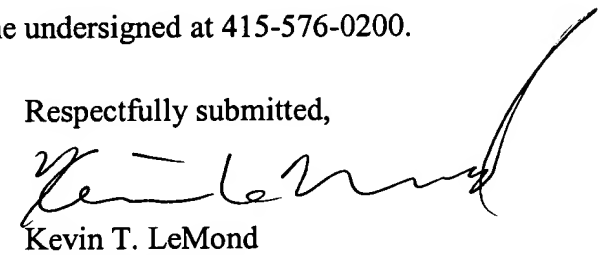
CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 415-576-0200.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

6. (New) A wafer for use in making a chip device, the wafer comprising:

a non-passivated die;

a first titanium layer at non-isolation locations on the die;

a first copper layer directly on the first titanium layer;

a titanium passivation layer directly on the first copper layer at non-solder bump locations; and

under bump material directly on the first copper layer at solder bump locations.

7. (New) A wafer in accordance with claim 6 further comprising solder bumps on the under bump material.

8. (New) A chip device comprising:

a non-passivated die;

a first titanium layer at non-isolation locations on the die;

a first copper layer directly on the first titanium layer;

a titanium passivation layer directly on the first copper layer at non-solder bump locations; and

under bump material directly on the first copper layer at solder bump locations.

9. (New) A chip device in accordance with claim 8 further comprising solder bumps on the under bump material